In the Claims

1-21. (Canceled)

22. (Previously Presented) A memory circuit, comprising:

control logic for providing a selected mode control signal;

selection and temporary storage circuitry for receiving and storing a first external address; and

a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching the memory circuit between a burst mode and a pipelined mode.

23. (Previously Presented) A memory circuit, as in Claim 22, wherein the control logic is adapted to receive an external mode select signal for selecting the burst mode or the pipelined mode and for determining the selected mode control signal.

24. (Original) A memory circuit, as in Claim 22, wherein the control logic includes mode circuitry for providing the selected mode control signal, the mode circuitry coupled for receiving an enable signal for determining the selected mode control signal.

25. (Original) A memory circuit, as in Claim 24, wherein the enable signal is selected from a group consisting of write enable and output enable signals.

26. (Original) A memory circuit, as in Claim 22, wherein the selection and temporary storage circuitry is coupled to a counter.

27. (Original) A memory circuit, as in Claim 26, wherein the counter is used for incrementing the first external address when in the burst mode.

28. (Original) A memory circuit, as in Claim 26, wherein the selection and temporary storage circuitry is coupled for receiving the first external address and a second external address subsequent thereto for operating in the pipelined mode.

29. (Original) A memory circuit, as in Claim 28, wherein the pipelined mode and the burst mode are extended data out modes.

30. (Original) A memory circuit, as in Claim 29, wherein the pipelined mode and the burst mode have no column address strobe cycle latency during a write cycle.

31. (Original) A memory circuit, as in Claim 30, wherein the pipelined mode and the burst mode have at least a two column address strobe cycle latency during a read cycle.

32. (Previously Presented) A memory circuit, as in Claim 26, wherein the memory circuit is incorporated in an asynchronously-accessible random access memory.

33-58. (Canceled)

59. (Previously Presented) A memory circuit, comprising:

control logic for providing a selected mode control signal;

selection and temporary storage circuitry for receiving and storing a first external address; and

a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching the memory circuit between a burst mode and a pipelined mode, wherein the memory circuit is an asynchronous dynamic random access memory circuit.

60. (Canceled)

61. (Canceled)

62. (Canceled)

63. (Currently Amended) A memory circuit, comprising:

control logic for providing a selected mode control signal;

selection and temporary storage circuitry for receiving and storing a first and a second external address;

a first multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom;

a second multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the second external address and the selected mode control signal respectively therefrom, wherein each multiplexer selects its respective external address when the selected mode control signal indicates a pipeline mode, and each multiplexer selects a supplied internal address when the selected mode control signal indicates a burst ~~pipelined~~ mode.

64. (Original) The memory circuit of claim 63, and further comprising:

a counter connected between the control logic and the first and second multiplexers, and operatively connected to receive the first and second external address signals, the counter generating a count 0 and a count 1 signal supplied to the first and second multiplexers, respectively, wherein the count 0 and count 1 signals are selected by the first and second multiplexers when the selected mode control signal indicates a burst mode.

65. (Original) A memory circuit, comprising:

control logic for providing a mode signal indicating a pipelined mode or a burst mode of operation;

selection and temporary storage circuitry for receiving and storing a first and a second external address;

a counter connected to the control logic, and coupled to receive the first and the second

external address, the counter generating count 0 and count 1 signals; and

a pair of multiplexers, each multiplexer coupled to the selection and temporary storage circuitry, to the counter, and to the control logic, the first multiplexer for receiving the first external address, the count 0 signal, and the selected mode control signal respectively therefrom, and the second multiplexer for receiving the second external address, the count 1 signal, and the selected mode control signal respectively therefrom, the multiplexers selecting the count 0 and count 1 signals when the mode control signal indicates a burst mode, and selecting the first and second external address signals when the mode control circuitry indicates a pipelined mode.

66. (Previously Presented) A memory circuit, comprising:

control logic for providing a selected mode control signal;

selection and temporary storage circuitry for receiving and storing a first external address; and

a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching the memory circuit from a pipelined mode to a burst mode.

67. (Previously Presented) The memory circuit of Claim 66, wherein the control logic is adapted to receive an external mode select signal for selecting the burst mode and for determining the selected mode control signal.

68. (Previously Presented) The memory circuit of Claim 66, wherein the control logic includes mode circuitry for providing the selected mode control signal, the mode circuitry coupled for receiving an enable signal for determining the selected mode control signal.

69. (Previously Presented) The memory circuit of Claim 68, wherein the enable signal is a write enable signal.

70. (Previously Presented) The memory circuit of Claim 68, wherein the enable signal is an output enable signal.

71. (Previously Presented) The memory circuit of Claim 66, wherein the selection and temporary storage circuitry is coupled to a counter, and wherein the counter is used for incrementing the first external address when in the burst mode.

72. (Previously Presented) The memory circuit of Claim 66, wherein the pipelined mode and the burst mode are extended data out modes.